Title	***Engineering Prototype Report (EP-21) – 30 W DC-DC Converter with DPA424***
Specification	36 VDC to 72 VDC Input, 5 V @ 6 A Output
Application	Telecom
Author	PI Applications Department
Document Number	EPR-21
Date	19-Nov-02
Revision	4.0

Features

- Very Low Component Count
- High Efficiency
  - No current sense components
  - Integrated MOSFET designed for very low switching and gate drive losses
  - 85% with low cost S.B.D. rectifier
- *DPA-Switch* Integrates:
  - Accurate line OV and OV shutdown
  - Thermal protection
  - Overload and open loop fault protection
  - Regulation at zero load (cycle skipping)
  - 400 kHz trimmed internal oscillator
- No Heat Sink or Derating at up to 55 °C
- Tested Over Industrial Temperature Range (-40 °C to 85 °C)
- High Bandwidth (6 kHz)

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Important Note:
Although the EP-21 is designed to satisfy telecom safety isolation requirements, this engineering prototype has not been agency approved.

1 Introduction

This document is an engineering report describing a 5 V, 30 W DC-DC converter utilizing the DPA424R.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

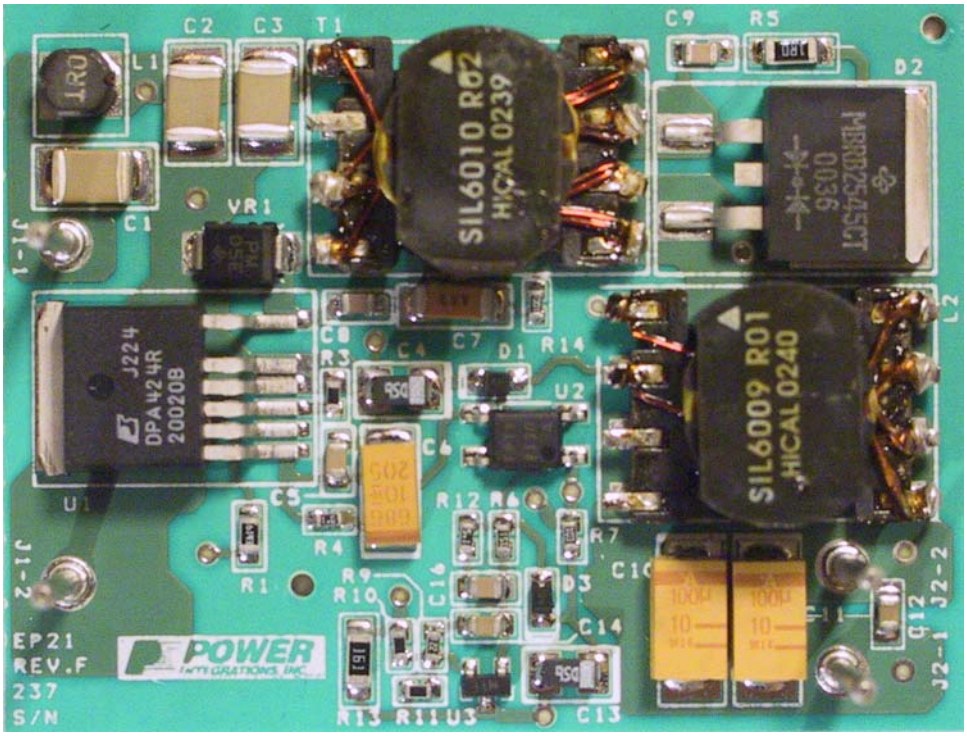

Figure 1 – EP-21 Populated Circuit Board (57.5 mm L x 43.6 mm W x 10.7 mm H).

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Input Voltage	V_{IN}	36	48	72	VDC	
Input Voltage UV Turn-On				36	VDC	See AN-31
Input Voltage UV Turn-Off		29			VDC	See AN-31
Input Voltage OV Turn-Off		75		90	VDC	See AN-31
Input Voltage OV Turn-On		72			VDC	See AN-31
Output						
Output Voltage	V_{OUT}	4.8	5	5.2	V	± 4%
Output Ripple and Noise	V_{RIPPLE}		65	100	mV	20 MHz Bandwidth
Output Current	I_{OUT}	0		6	A	
Line Regulation				± 0.2	%	
Load Regulation				± 0.5	%	
Transient Response Peak Deviation			3		% of V_{OUT}	50% to 75% load step, 100 mA/µs di/dt, 48 VDC input
Transient Response Recovery			200		µs	To 1% of final output voltage, 50% to 75% load step, 48 VDC input
Overload Current	I_{OUT_OL}			8	A	Unit enters auto-restart
Total Output Power						
Continuous Output Power	P_{OUT}			30	W	
Efficiency	η		85		%	Measured at P_{OUT} (30 W), 25 °C, 48 VDC Input
Environmental						
Input-Output Isolation Voltage		1500			VDC	
Ambient Temperature	T_{AMB}	-40		75	°C	Maximum continuous output power, 110 °C base plate temperature, natural convection, with Wakefield 628-65AB heat sink
Dimensions					mm	57.5 mm L x 43.6 mm W x 10.7mm H (16.8 mm H including pins)

3 Schematic

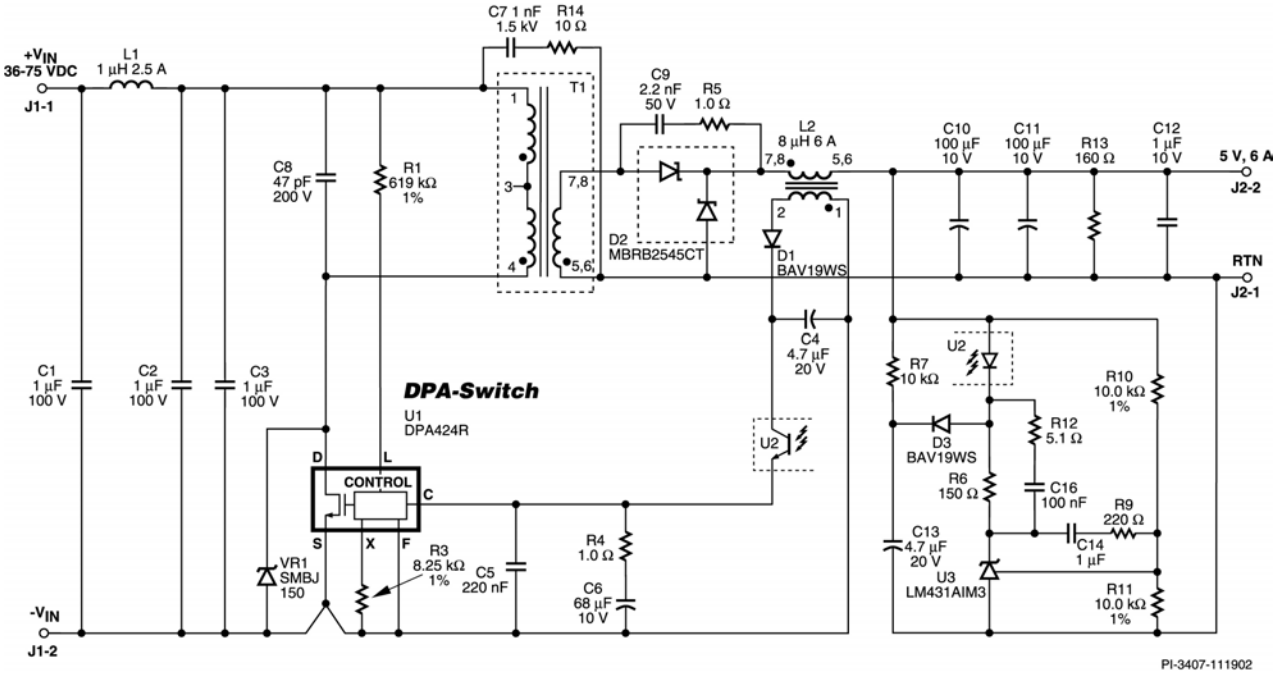

Figure 2 – EP-21 Schematic.

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4 Circuit Description

4.1 Primary Circuitry

The schematic in Figure 2 shows a single-ended forward converter using the DPA424R. The circuit is designed for 36 V to 72 V input range and 5 V, 6 A output. C1 and L1 provide input filtering. C2 and C3 bypass the DC rail. The DC rail is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. C8 reduces the amplitude of leakage spikes generated when the MOSFET in U1 switches off. VR1 clamps the U1 drain voltage to a safe value during fault conditions, but is inactive during normal operation.

R1 is used to set the low line turn-on threshold to approximately 33 V, and also sets the overvoltage shutdown level to approximately 88 V. R3 sets the U1 current limit to approximately 85% of its nominal value, limiting the output power delivered during fault conditions. C5 bypasses the U1 CONTROL pin, and provides the peak current necessary for driving the *DPA-Switch* internal MOSFET. C6 has three functions. It provides the energy required by U1 during startup, sets the auto-restart frequency during fault conditions, and also reduces the gain of U1 as a function of frequency. R4 adds a zero to stabilize the power supply control loop.

4.2 Output Rectification

The output of T1 is rectified and filtered by D2, L2, C10, and C11. This is the lowest cost rectification scheme. *DPA-Switch* is however fully compatible with simple self-driven synchronous rectification schemes as described in the *DPA-Switch* datasheet. C12 provides additional high frequency filtering, and is located close to the output terminals of the supply. C7 provides bypassing for high frequency common-mode noise coupled from the primary to the secondary of T1. R14 damps primary-to-secondary circulating current, which would otherwise appear imposed on the output ripple voltage.

C9 and R5 provide some snubbing to D2, but their main purpose is to reset T1 during the U1 off time. During the U1 off time, magnetizing energy stored in the T1 primary during on time is coupled to the secondary, and charges C9. The voltage on C9 is a 1/2 sinusoid with a period determined by C9 and the reflected primary inductance of T1. C9 is sized such that the voltage generated during the off time is sufficient to reset T1 before the next switching cycle occurs. R5 provides damping for C9 to prevent high frequency ringing during switching transitions.

U1 is powered during normal operation by an auxiliary flyback winding on L2. This winding delivers energy during the off time of U1, with an output voltage proportional to the supply output voltage. The turns ratio of L2 sets the output voltage of the auxiliary winding to approximately 12 V. D1 and C4 rectify and filter the auxiliary winding output.

R13 applies a small amount of preloading to the supply output to prevent the voltage at the auxiliary winding of L1 from collapsing at zero load. R13 is set to provide a minimum of 8 V at the cathode of D1 at zero load.

4.3 Output Feedback

R10 and R11 divide down the supply output voltage and apply it to the reference pin of error amplifier U3. U3 drives optocoupler U2 through resistor R6 to provide feedback information to the CONTROL pin of U1. The optocoupler output also provides power to U1 during normal operating conditions. D3 and C13 apply drive to the optocoupler during supply startup to eliminate output voltage overshoot. D3 isolates C13 from the supply feedback loop after startup. R7 discharges C13 when the supply is off. R8 provides bias current to U3.

C6, C14, C16, R4, R6, R9, and R12 all play a role in compensating the power supply control loop. C6 rolls off the gain of U1 at a relatively low frequency. R4 provides a zero to cancel the phase shift of C6. R6 sets the gain of the direct signal path from the supply output through U2 and U3. C14 and R9 roll off the gain of U3. R12 and C16 provide phase boost near the output filter (L2, C10-11) resonant frequency to improve phase margin and stability.

4.4 Construction

The EP21 is constructed with surface mount components using an aluminum clad circuit board. The printed circuit board is an effective heat spreader, and allows attachment of a heat sink on the back of the board for operation at high ambient temperature. Tantalum and ceramic capacitors are used instead of conventional electrolytic capacitors to enable operation at extreme ambient temperatures.

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5 PCB Layout

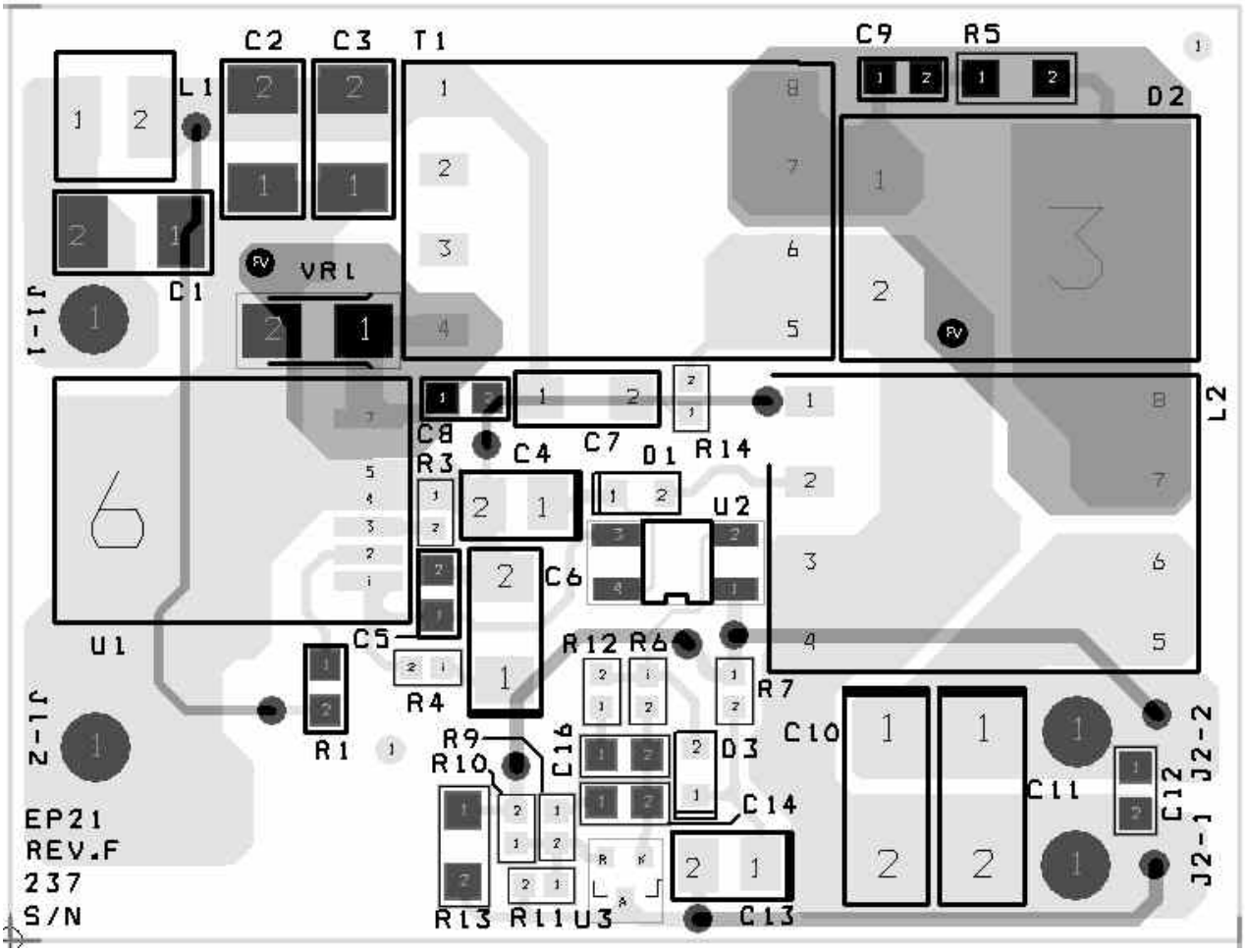

Figure 3 – EP-21 Printed Circuit Layout.

6 Bill Of Materials

EP-21 30 W 400 kHz DC-DC
Bill Of Materials

Item	Qty	Reference	Description	P/N	Manufacturer
1	3	C1-3	1 μF, 100 V 1812	THCR50E2A105ZT	UCC
2	2	C4, 13	4.7 μF, 20 V B size	ECS-T1DY475R	Panasonic
3	2	C5	220 nF, 25 V 0805	ECJ-2VB1C224K	Panasonic
4	1	C6	68 μF, 10 V tantalum C size	T491C476K010	Kemet
5	1	C7	1 nF, 1.5 kV 1808	1808SC102KAT1A	AVX
6	1	C8	47 pF, 200 V 0805	ECJ-2VC2D470J	Panasonic
7	1	C9	2.2 nF, 50 V 0805	ECJ-2VB1H222K	Panasonic
8	2	C10, 11	100 μF, 10 V tantalum	TPSD10710R0100	AVX
9	2	C12, 14	1 μF, 10 V 0805	ECJ-2YB1A105K	Panasonic
10	1	C16	100 nF, 25 V 0805	ECJ-2YB1E104K	Panasonic
11	2	D1, 3	250 mA, 100 V SOD-323	BAV19WS	Diodes, Inc.
12	1	D2	Schottky 25 A, 45 V	MBRB2545CT	General Semiconductor
13	1	L1	1 μH, 2.5 A	SCD-0403-1R0M	Chilisin
14	1	L2	8 μH, 6 A PR1408	SIL6009 Rev. 6	HiCal
15	1	R1	619 kΩ, 1% 0805	ERJ-6ENF6193V	Panasonic
16	1	R2	Not Placed		
17	1	R3	8.25 kΩ, 1% 0603	ERJ-3EKF8251V	Panasonic
18	1	R4	1 Ω, 5% 0603	ERJ-3GEYJ1R0V	Panasonic
19	1	R5	1 Ω, 5% 1206	ERJ-8GEYJ1R0V	Panasonic
20	1	R6	150 Ω, 5% 0603	ERJ-3GEYJ151V	Panasonic
21	1	R7	10 kΩ, 5% 0603	ERJ-3GEYJ103V	Panasonic
22	1	R8	1 kΩ, 5% 0603	ERJ-3GEYJ102V	Panasonic
23	1	R9	220 Ω, 5% 0603	ERJ-3GEYJ221V	Panasonic
24	2	R10, 11	10 kΩ, 1% 0603	ERJ-3EKF1002V	Panasonic
25	1	R12	5.1 Ω, 5% 0603	ERJ-3GEYJ5R1V	Panasonic
26	1	R13	160 Ω, 5% 1206	ERJ-8GEYJ161V	Panasonic
27	1	R14	10 Ω, 5% 0603	ERJ-3GEYJ100V	Panasonic
28	1	R15	Not Placed		
29	1	T1	Transformer, Custom, PR1408	SIL6010 Rev. 8	HiCal
30	1	U1	DPA424R		Power Integrations
31	1	U2	Optocoupler, graded CTR	PC357N1T	Sharp
32	1	U3	Shunt Regulator SOT-23	LM431AIM3	National Semiconductor
33	1	VR1	TVS 150 V, 600 W	SMBJ150A	General Semiconductor
34	4	J1-1, 2 J2-1, 2	Pin, Surface Mount, 0.060” x 0.580”	1248-580-6	Zierick
35	1		EP-21 Aluminum Clad Printed Circuit Board Rev. E		

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7 Transformer Specification

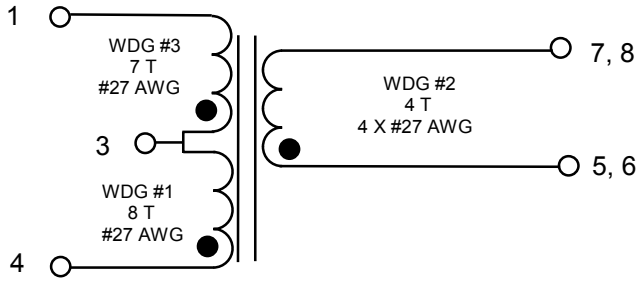

Figure 4 – EP-21 Transformer.

7.1 Electrical Specifications

Electrical Strength	1 s, from Pins 1-4 to Pins 5-8	1500 VDC
Creepage	Between Pins 1-4 and Pins 5-8	N/A
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 400 mV_{RMS}	450 µH, ±25%
Resonant Frequency	Pins 1-4, all other windings open	3.8 MHz (min.)
Primary Leakage Inductance	Pins 1-4, with Pins 5-8 shorted, measured at 100 kHz, 400 mV_{RMS}	1 µH (max.)

7.2 Materials

Item	Description
[1]	Core: PR 14 X 8 Ungapped N87 Material Epcos P/N B65755-J-R87
[2]	Bobbin: 8 pin P1408 surface mount B&B B-096 or equivalent
[3]	Magnet Wire: #27 AWG Double Coated
[4]	Tape, Polyester, 3M #1298 or equiv. 4.5 mm wide
[5]	Varnish

7.3 Transformer Build Diagram

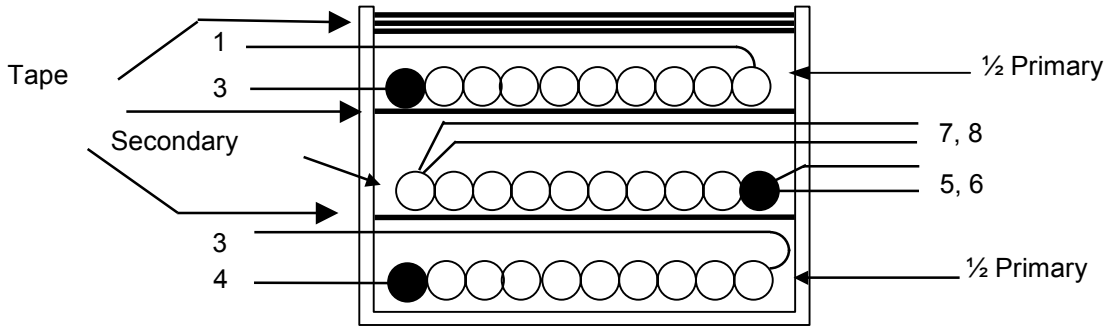

Figure 5 – EP-21 Transformer Build Diagram.

7.4 Transformer Construction

½ Primary	Start at Pin 4. Wind 8 turns of item [3] in 1 layer. Finish on Pin 3.
Basic Insulation	Use one layer of item [4] for basic insulation.
Secondary Winding	Start at Pins 5 and 6. Wind 4 quadrifilar turns of item [3]. Finish on Pins 7 and 8.
Basic Insulation	Use one layer of item [4] for basic insulation.
½ Primary	Start at Pin 3. Wind 7 turns of item [3] in 1 layer. Finish on Pin 1.
Outer Wrap	Wrap windings with 3 layers of tape item [4].
Final Assembly	Assemble and secure core halves. Varnish impregnate item [5].

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8 Inductor Specification

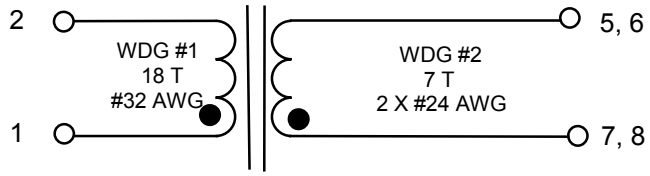

Figure 6 – EP-21 Inductor, L2 Rev. 6.

8.1 Electrical Specifications

Electrical Strength	1 s, from Pins 1, 2 to Pins 5-8	1500 VDC
Creepage	Between Pins 1, 2 and Pins 5-8	N/A
Inductance	Pins 5, 6 to 7, 8, all other windings open, measured at 100 kHz, 400 mV_{RMS}	8 μH, ±10%
Resonant Frequency		N/A
Primary Leakage Inductance		N/A

8.2 Materials

Item	Description
[1]	Core: PR 14 X 8 Epcos N87, P/N B65755-J-R87 Gap for A_L of 163 nH/T^2
[2]	Bobbin: 8 pin P1408 surface mount B&B B-096 or equivalent
[3]	Magnet Wire: #24 AWG Double Coated
[4]	Magnet Wire: #32 AWG Double Coated
[5]	Tape, Polyester, 3M #1298 or equiv. 4.5 mm wide
[6]	Varnish

8.3 Inductor Build Diagram

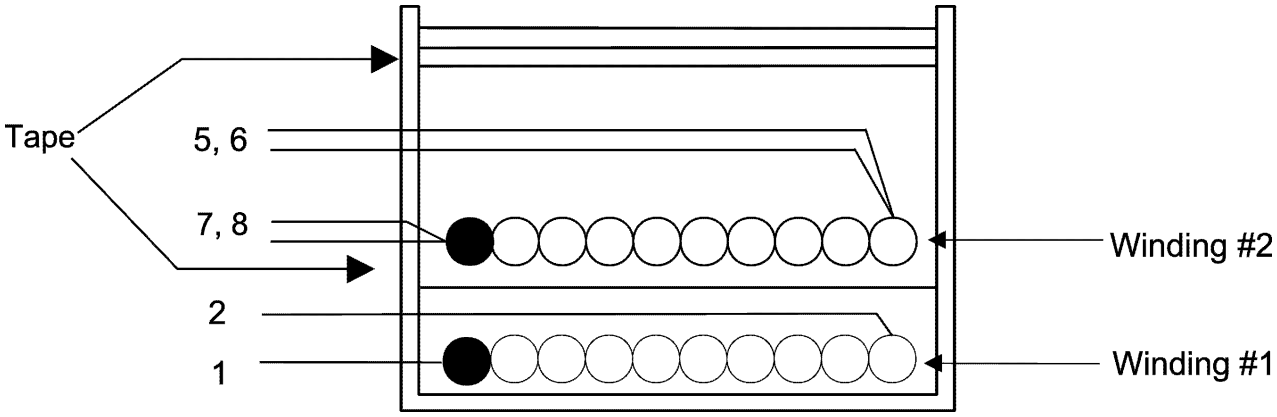

Figure 7 – EP-21 Inductor Construction.

8.4 Inductor Construction

Winding #1	Start at Pin 1. Wind 18 turns of item [4] in approximately 1 layer. Finish on Pin 2.
Basic Insulation	Use one layer of item [5] for basic insulation.
Winding #2	Start at Pins 7 and 8. Wind 7 bifilar turns of item [3]. Finish on Pins 5 and 6.
Outer Wrap	Wrap windings with 3 layers of tape item [5].
Final Assembly	Assemble and secure core halves. Varnish impregnate item [6].

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9 PIXIs Design Spreadsheet

DCDC_DPAFwd_rev1.02_061802 Copyright Power Integrations Inc. 2002	INPUT	INFO	OUTPUT	UNIT	DPA_061802_R102xls: DPA-Switch Forward Transformer Design Spreadsheet
OUTPUT VOLTAGE AND CURRENT					**EP21 DC-DC Converter**
VMAIN	5			Volts	Main output voltage
IMAIN	6			Amps	Main output current
VOUT2				Volts	Output2 voltage
IOUT2				Amps	Output2 current
POUT			**30**	Watts	Total output power
VBIAS	12.0			Volts	DC bias voltage from output inductor winding
INPUT VOLTAGE AND UV/OV					
VMIN	36			DC volts	Minimum DC input voltage
VMAX	72			DC volts	Maximum DC input voltage
		min	max		
VUV OFF	30	30.0	33.1	DC volts	Minimum undervoltage On-Off threshold
VUV ON		32.2	34.6	DC volts	Maximum undervoltage Off-On threshold (turn-on)
VOV ON		74.8	-	DC volts	Minimum overvoltage Off-On threshold
VOV OFF		-	94.6	DC Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			618.0	kOhm	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series
ENTER DPA-Switch VARIABLES					
DPA-Switch	**dpa424**			*16VDC*	*36VDC*
Chosen Device	*DPA424*		*Power*	15.5 W	35W
ILIMIT	*2.32*	*2.68*		Amps	From DPA-Switch datasheet
Frequency - (F)=400kHz, (L)=300kHz	**f**				Full (F) frequency option - 400 kHz
fS	*375000*	*425000*	*400000*	Hertz	From DPA-Switch datasheet
KI	1				External limit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITEXT			2.32	Amps	External current limit
RX			-	kOhm	Current Limit resistor value (X-pin) - assumes minimum datasheet curve (fig 32)
DUVON GOAL			**0.71**		Maximum allowed duty cycle at VUV ON MIN undervoltage threshold
KDI			**0.15**		Maximum current ripple factor
VDS			2	Volts	DPA-Switch average on-state Drain to Source Voltage
VDSOP			**178.7**	Volts	Required drain voltage for guaranteed transformer reset
DIODE Vf SELECTION					
VDMAIN			0.5	Volts	Main output diodes forward voltage drop
VDOUT2			0.5	Volts	Secondary output diodes forward

					voltage drop
VDB			0.7	Volts	Bias diode forward voltage drop
TRANSFORMER CORE SELECTION					
Core Type	**pr14x8**				
Core		*PR14x8*		*P/N:*	*B65755-J-R87*
Bobbin		*PR14x8_Bo*		*P/N:*	*B65542-B-T1*
AE			0.253	cm^2	Core Effective Cross Sectional Area
LE			2.53	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			4.4	mm	Bobbin Physical Winding Width
LG MAX	0.005		0.005	mm	Maximum actual gap when zero gap specified
D FACTOR			1.00		Duty cycle factor
L	1.10				Transformer primary layers (split primary recommended)
NMAIN			4		Main rounded turns
NS2			0		Vout2 rounded secondary turns (AC stacked winding)
VOUT2 ACTUAL			0.0	Volts	Approximate Output2 voltage of with NS2 = 0 turns (AC stacked secondary)
TRANSFORMER DESIGN PARAMETERS					
NP			15		Primary rounded turns
BM			**1449**	Gauss	Max operating flux density at minimum switching frequency
BP			**2794**	Gauss	Max transient flux density at minimum switching frequency
LP MIN			0.342	mHenries	Minimum primary magnetizing inductance (assumes LG MAX-5um)
IMAG			0.151	Amps	Peak magnetizing current at minimum input voltage
OD_P			0.38	mm	Primary wire outer diameter
AWG_P			**27**	AWG	Primary Wire Gauge (rounded to maximum AWG value)
DUTY CYCLE VALUES					
DUVON MIN			**0.68**		Duty cycle at minimum undervoltage threshold
DVMIN			0.61		Duty cycle at minimum DC input voltage
DVMAX			0.29		Duty cycle at maximum DC input voltage
DOVOFF MAX			0.22		Duty cycle at maximum DC overvoltage threshold
CURRENT WAVESHAPE PARAMETERS					
IP			**1.835**	Amps	Maximum peak primary current at maximum DC input voltage
IPRMS			1.246	Amps	Maximum primary RMS current at minimum DC input voltage
COUPLED INDUCTOR OUTPUT PARAMETERS					
LMAIN	8		8.0	uHenries	Main / Output2 coupled output inductance (referred to Main winding)
WLMAIN			144	uJoules	Main / Output2 coupled inductor full-load stored energy

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KDIMAIN			0.20		Current ripple factor of combined Main and Output2 outputs
nOUT2			0.0		Approximate turns ratio for Output2 winding
nBIAS			2.3		Approximate turns ratio for Bias winding
SECONDARY OUTPUT PARAMETERS					*No derating*
ISMAINRMSLL			4.67	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
ISOUT2RMSLL			0.00	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
IDAVMAIN			4.23	Amps	Maximum average current, Main rectifier (single device rating)
IDAVOUT2			0.00	Amps	Maximum average current, Main rectifier (single device rating)
IRMSMAIN			0.35	Amps	Maximum RMS current, Main output capacitor
IRMSOUT2			0.00	Amps	Maximum RMS current, Out2 output capacitor
VPIVMAIN			39.6	Volts	Main rectifiers peak-inverse voltage
VPIVOUT2			0.0	Volts	Output2 rectifiers peak-inverse voltage
VPIVB			58.1	Volts	Bias output rectifier peak-inverse voltage

10 Performance Data

All measurements performed at room temperature unless otherwise specified.

10.1 Efficiency

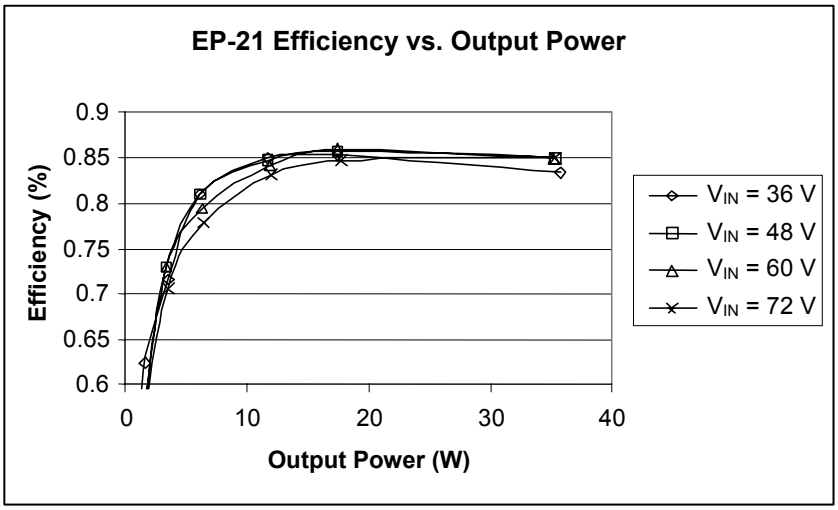

Figure 8 – Efficiency vs. Output Power, Room Temperature.

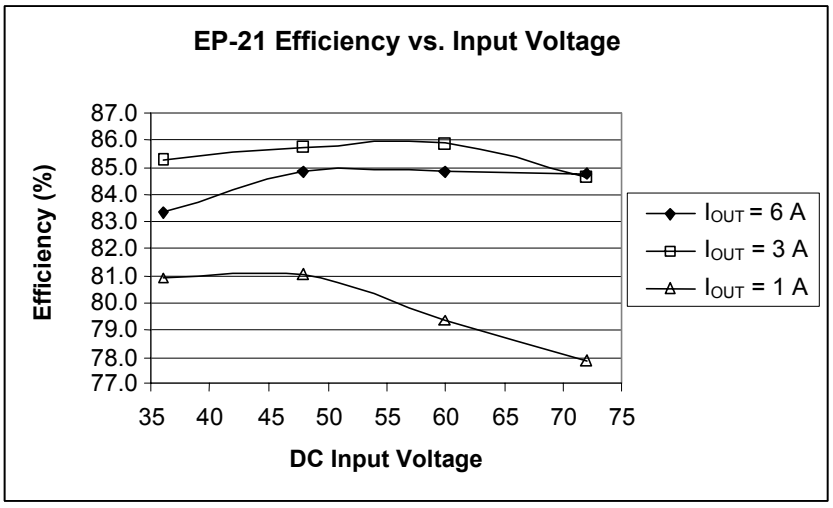

Figure 9 – Efficiency vs. Input Voltage, Room Temperature.

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10.2 Regulation

10.2.1 Load Regulation

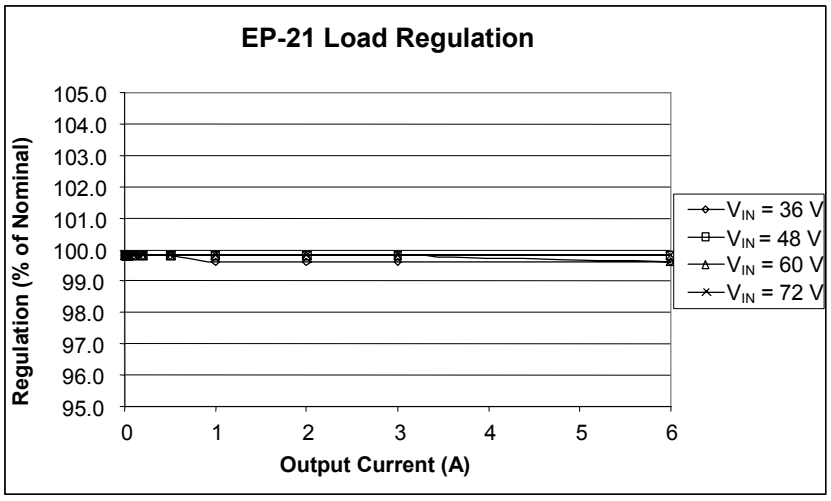

Figure 10 – Load Regulation, Room Temperature.

10.2.2 Line Regulation

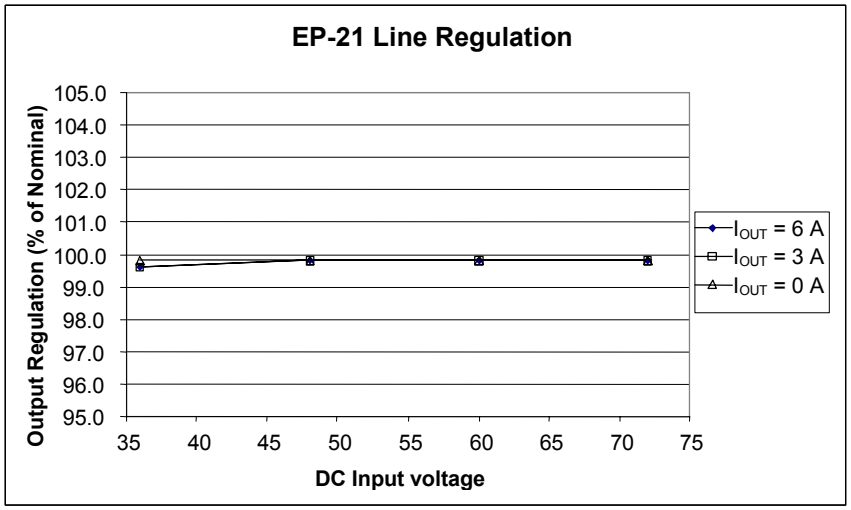

Figure 11 – Line Regulation, Room Temperature.

11 Thermal Performance

Thermal performance of the EP-21 was measured in still air at room temperature with no heat sink and with a Wakefield 628-65AB heat sink attached to the aluminum substrate using Berquist Bond Ply 105 thermal adhesive. The supply was also tested in still air in a thermal chamber with the ambient temperature adjusted for 110 °C base plate temperature, both with and without a heat sink. The results are tabulated below.

Input Voltage	36 VDC	48 VDC	72 VDC
Item			
Ambient	25 °C	25 °C	25 °C
DPA-Switch (U1)	68 °C	64.5 °C	64 °C
Transformer (T1)	67 °C	64 °C	64 °C
Output Choke (L2)	67 °C	67 °C	68.5 °C
Output Rectifier (D2)	73 °C	71 °C	72 °C
Base Plate	66 °C	63 °C	62 °C

Figure 12 – EP-21 Thermal Performance with Attached Heat Sink, Room Temperature, Maximum Load.

Input Voltage	36 VDC	48 VDC	72 VDC
Item			
Ambient	76 °C	77 °C	82.5 °C
DPA-Switch (U1)	115° C	113° C	113 °C
Transformer (T1)	116 °C	115 °C	117 °C
Output Choke (L2)	112.5 °C	113 °C	118 °C
Output Rectifier (D2)	113 °C	113 °C	117 °C
Base Plate	110 °C	110 °C	110 °C

Figure 13 – EP-21 Thermal Performance with Attached Heat Sink, Ambient Temperature Adjusted for 110 °C Base Plate Temperature.

Input Voltage	36 VDC	48 VDC	72 VDC
Item			
Ambient	30 °C	30 °C	29 °C
DPA-Switch (U1)	87 °C	82 °C	80 °C
Transformer (T1)	86 °C	82 °C	81.5 °C
Output Choke (L2)	82 °C	80 °C	82 °C
Output Rectifier (D2)	95 °C	91 °C	90.5 °C
Base Plate	86 °C	81 °C	80 °C

Figure 14 – EP-21 Thermal Performance, No Heat Sink, Room Temperature, Maximum Load.

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Input Voltage	36 VDC	48 VDC	72 VDC
Item			
Ambient	57 °C	61 °C	69 °C
DPA-Switch (U1)	114 °C	113 °C	113 °C
Transformer (T1)	114.5 °C	115 °C	116 °C
Output Choke (L2)	110 °C	112 °C	115 °C
Output Rectifier (D2)	114 °C	115 °C	117 °C
Base Plate	110 °C	110 °C	110 °C

Figure 15 – EP-21 Thermal Performance, No Heat Sink, Maximum Load, Ambient Temperature Adjusted for 110 °C, Base Plate Temperature.

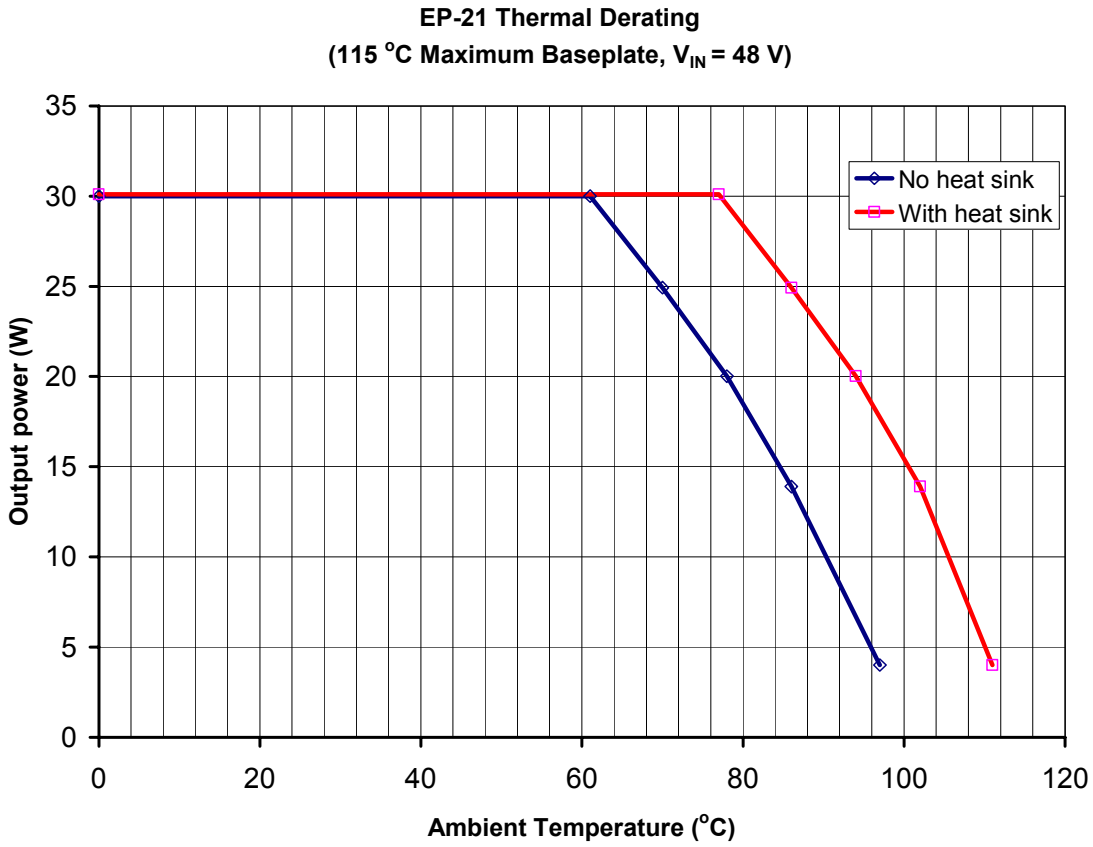

Figure 16 – EP-21 Output Power Thermal Derating.

12 Waveforms

12.1 Drain Voltage and Current, Normal Operation

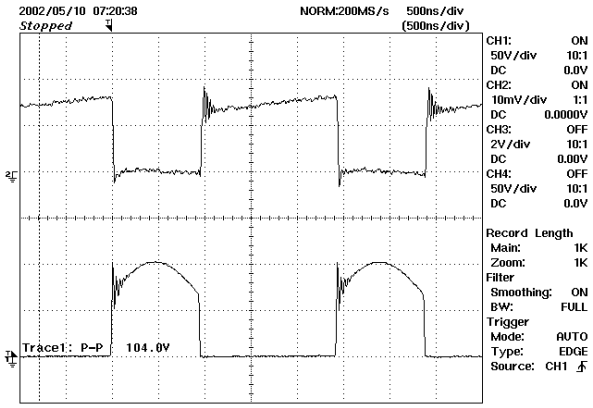

Figure 17 – 36 VDC, Full Load.
Upper Trace: I_{DRAIN}, 1 A/div.
Lower Trace: V_{DRAIN}, 50 V/div,
500 ns/div.

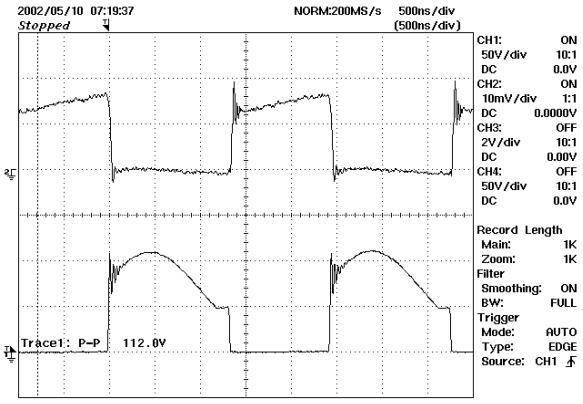

Figure 18 – 48 VDC, Full Load.
Upper Trace: I_{DRAIN}, 1 A/div.
Lower Trace: V_{DRAIN}, 50 V/div,
500 ns/div.

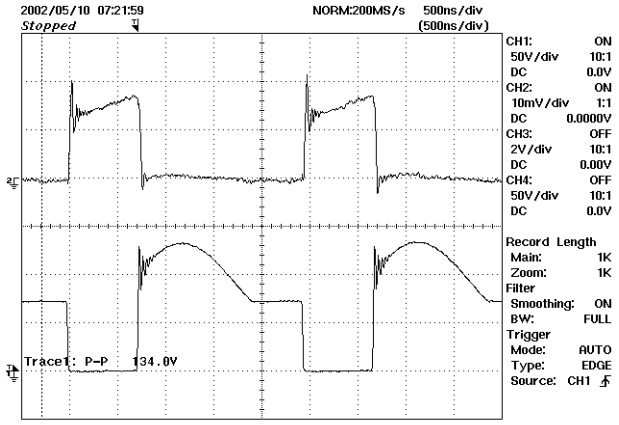

Figure 19 – 72 VDC, Full Load.
Upper Trace: I_{DRAIN}, 1 A/div.
Lower Trace: V_{DRAIN}, 50 V/div,
500 ns/div.

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12.2 Output Voltage Start-up Profile

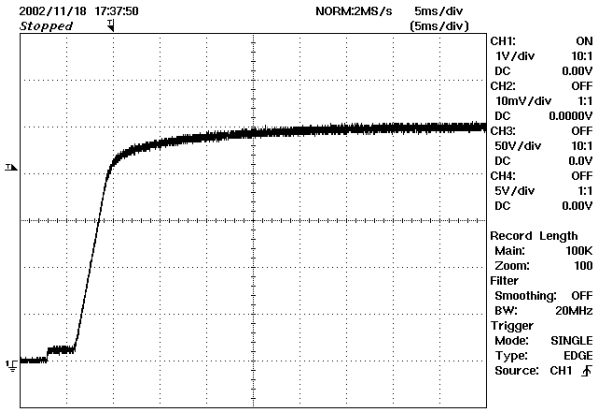

Figure 20 – Start-up Profile, 36 VDC, Full Load.
1 V/div, 5 ms/div.

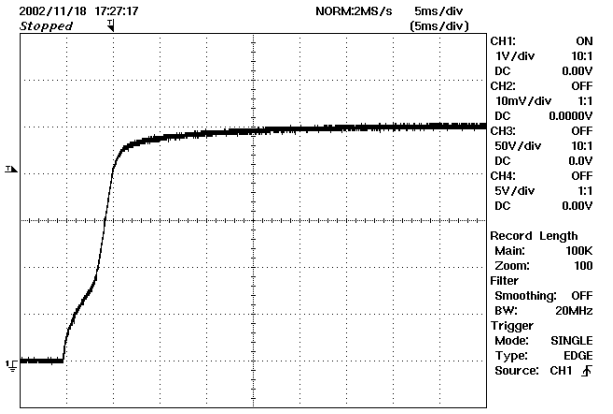

Figure 21 – Start-up Profile, 36 VDC, Zero Load.
1 V/div, 5 ms/div.

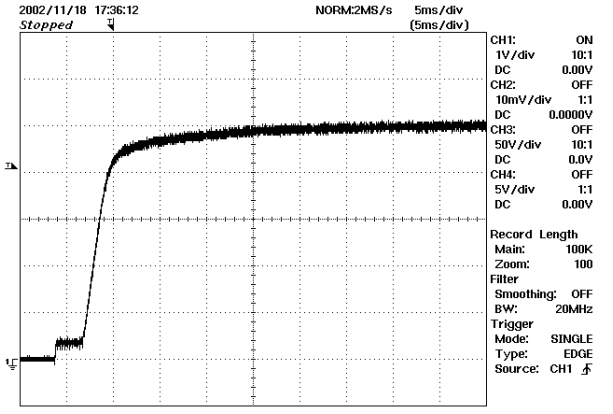

Figure 22 – Start-up Profile, 48 VDC, Full Load.
1 V/div, 5 ms/div.

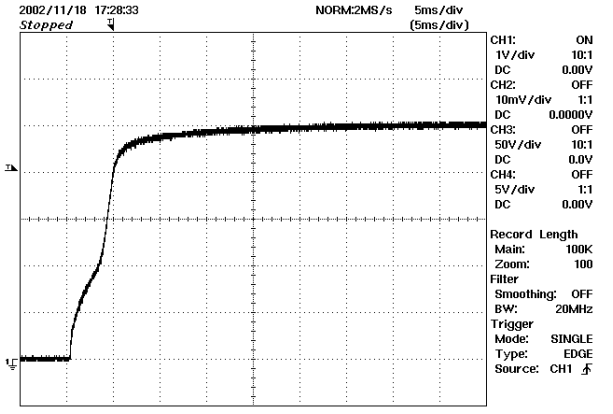

Figure 23 – Start-up Profile, 48 VDC, Zero Load.
1 V/div, 5 ms/div.

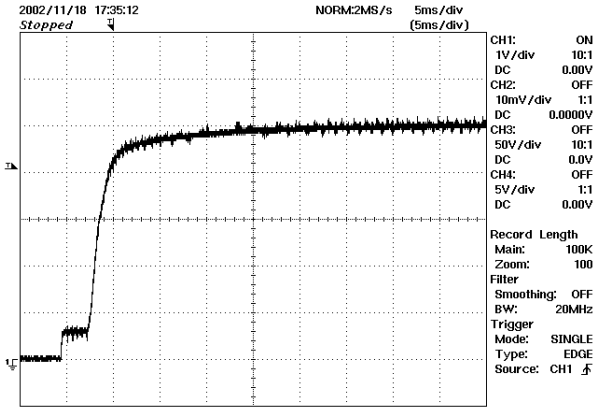

Figure 24 – Start-up Profile, 72 VDC, Full Load.
1 V/div, 5 ms/div.

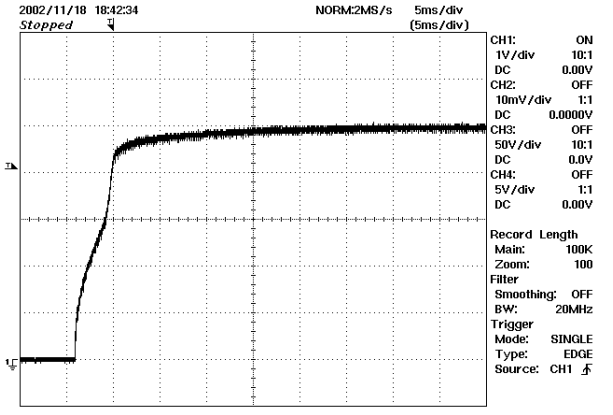

Figure 25 – Start-up Profile, 72 VDC, Zero Load,
1 V/div, 5 ms/div.

12.3 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output ripple occurs essentially at random with respect to the load transient, contributions to the displayed trace form the output ripple will average out, leaving the contribution only from the load step response.

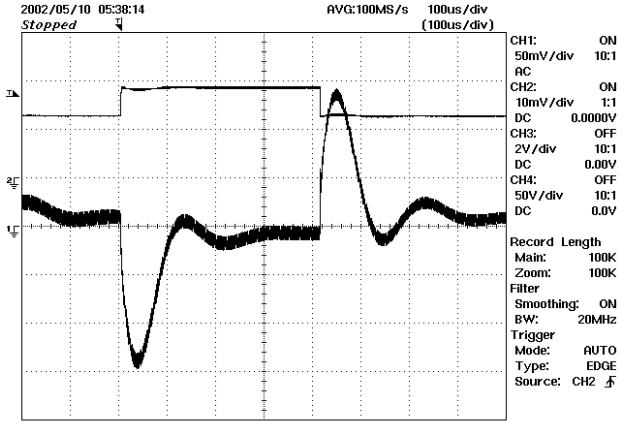

Figure 26 – Output Transient Response.
50% to 75% to 50% Load Step,
36 VDC Input.
Upper Trace: Load Current, 2 A/div.
Bottom Trace: Output Voltage,
50 mV/div, 100 μs/div.

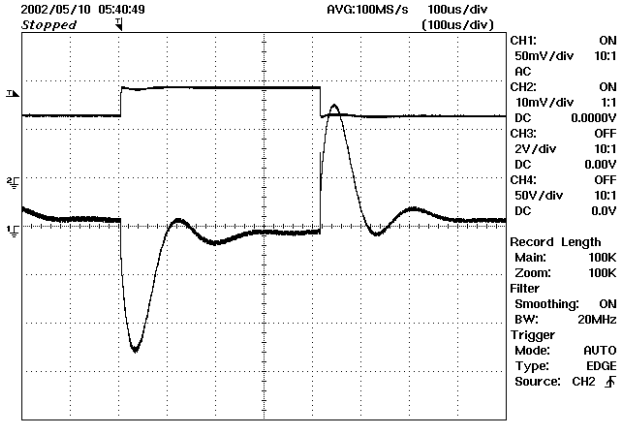

Figure 27 – Output Transient Response.
50% to 75% to 50% Load Step,
48 VDC Input.
Upper Trace: Load Current, 2 A/div.
Bottom Trace: Output Voltage,
50 mV/div, 100 μs/div.

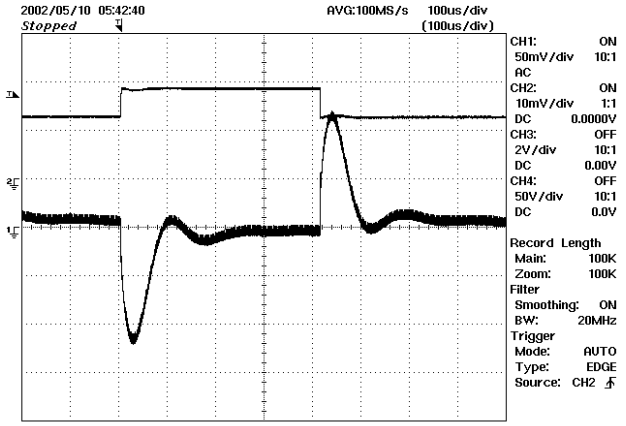

Figure 28 – Output Transient Response.
50% to 75% to 50% Load Step,
72 VDC Input.
Upper Trace: Output Current, 2 A/div.
Bottom Trace: Output Voltage,
50 mV/div, 100 μs/div.

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12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique
For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 29 and Figure 30.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF/50 V ceramic type and one (1) 1.0 µF/50 V aluminum electrolytic. *The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).*

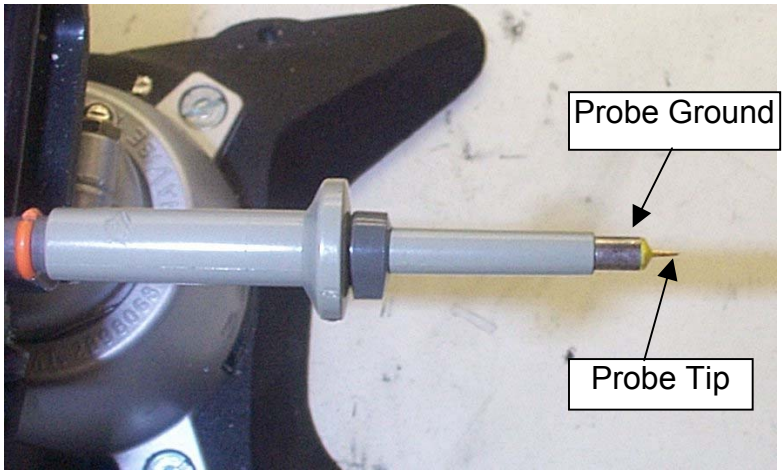

Figure 29 – Oscilloscope Probe Prepared for Ripple Measurement.
(End Cap and Ground Lead Removed).

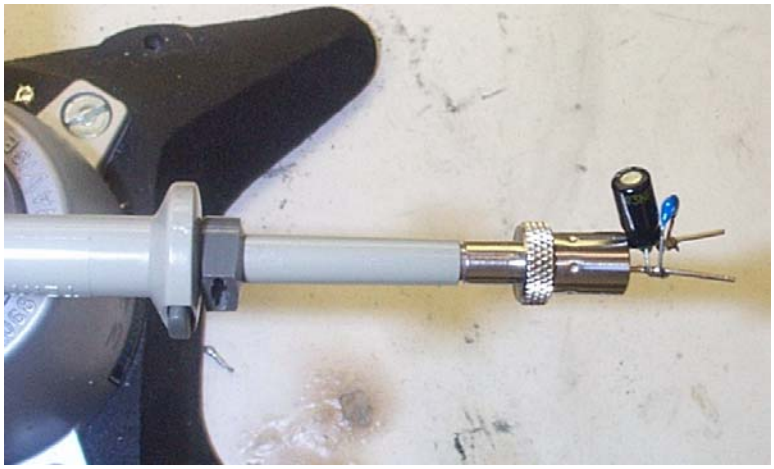

Figure 30 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter.
(Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

12.4.2 Measurement Results

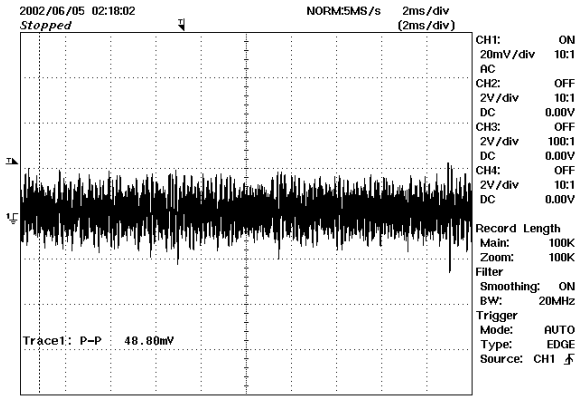

Figure 31 – Output Ripple, 36 VDC, Full Load, 2 ms/div, 20 mV/div.

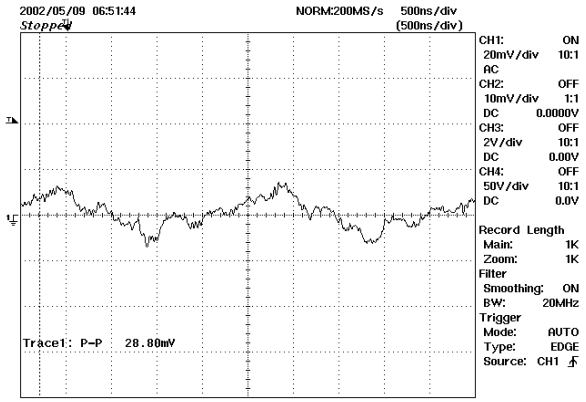

Figure 32 – Output Switching Frequency Ripple, 36 VDC, Full Load, 500 ns/div, 20 mV/div.

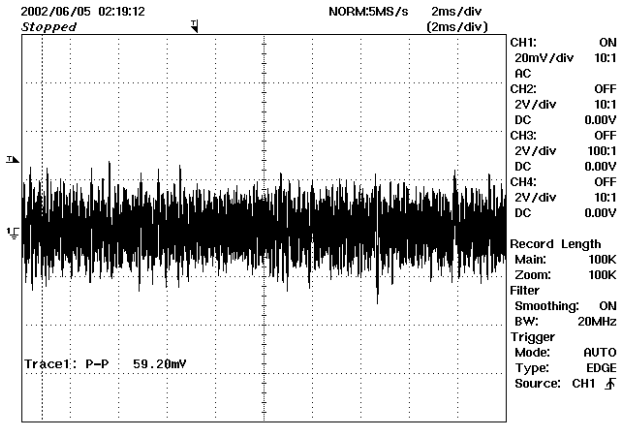

Figure 33 – Output Ripple, 48 VDC, Full Load, 2 ms/div, 20 mV/div.

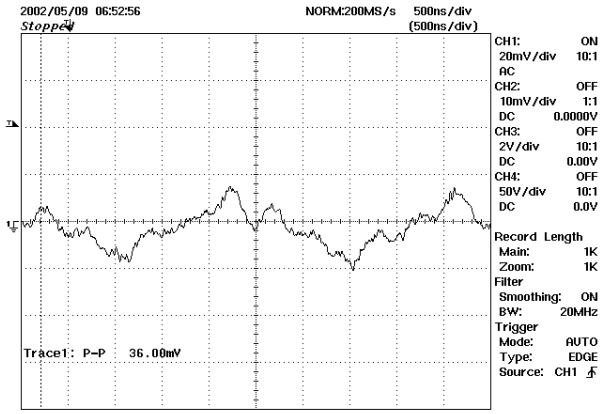

Figure 34 – Output Switching Frequency Ripple, 48 VDC, Full Load, 500 ns/div, 20 mV/div.

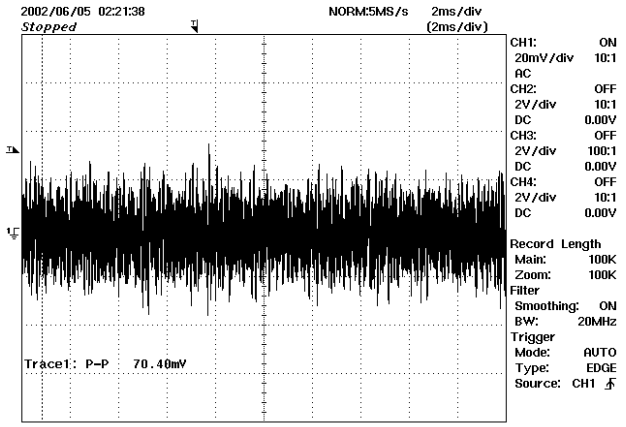

Figure 35 – Output Ripple, 72 VDC, Full Load, 2 ms/div, 20 mV/div.

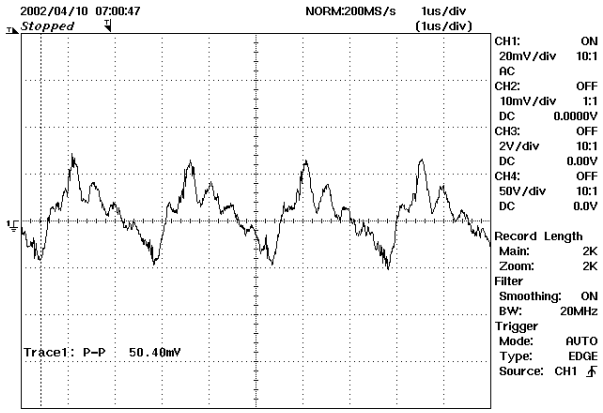

Figure 36 – Output Switching Frequency Ripple, 72 VDC, Full Load, 500 ns/div, 20 mV/div.

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13 Control Loop Measurements

13.1 Maximum Load 36 VDC

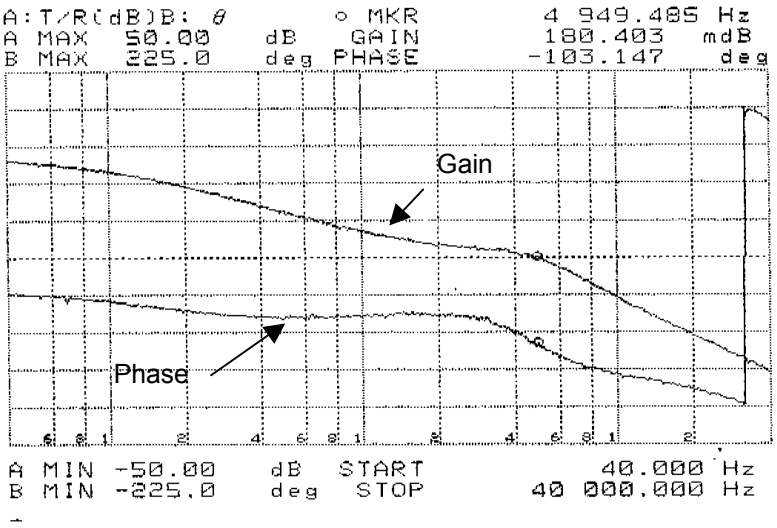

Figure 37 –Gain-Phase Plot, 36 VDC, Maximum Steady State Load.
Gain Crossover 4.94 kHz, Phase Margin 77°.

13.2 Maximum Load 48 VDC

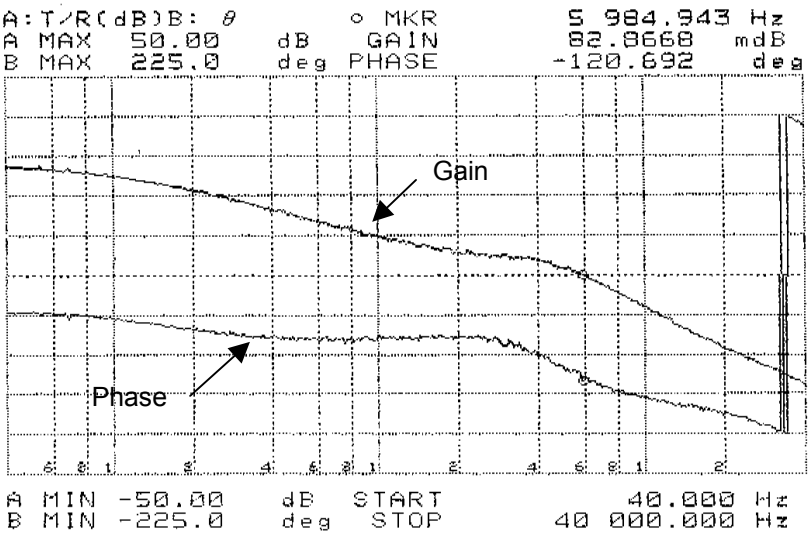

Figure 38 – Gain-Phase Plot, 48 VDC, Maximum Steady State Load.
Gain Crossover 5.98 kHz, Phase Margin 59.4°.

13.3 Maximum Load 72 VDC

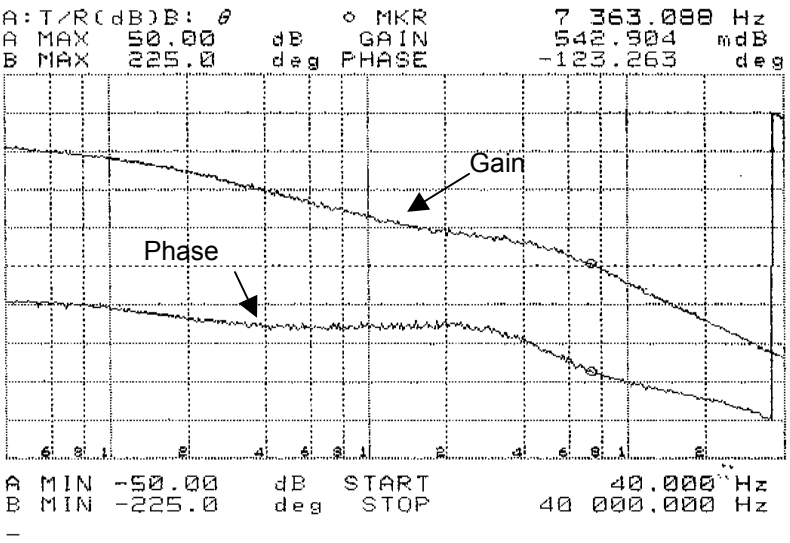

Figure 39 – Gain-Phase Plot, 72 VDC, Maximum Steady State Load.
Gain Crossover 7.36 kHz, Phase Margin 57°.

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14 Revision History

Date	Author	Revision	Description & changes
05-Jun-02	APP	1.0	First Release
10-Jul-02	APP	2.0	PIXIs Spreadsheet added
26-Sep-02	APP	3.0	Schematic updated
19-Nov-02	APP	4.0	Schematic, BOM, and start-up waveforms updated

Notes

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Notes

Notes

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